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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Levine et al.

§ Group Art Unit: 2192

Serial No.: 10/675,872

§ Examiner: Vo, Ted T.

Filed: September 30, 2003

§ Attorney Docket No.: AUS920030487US1

§

For: Method and Apparatus for
Counting Instruction and Memory
Location Ranges

Certificate of Mailing Under 37 C.F.R. § 1.8(a)

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By:

Louise Fay

35525

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By:

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Commissioner for Patents
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Alexandria, VA 22313-1450

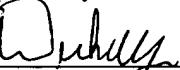
Sir:

ENCLOSED HEREWITH:

- Supplemental Information Disclosure Statement;
- Form PTO-1449;
- References AH-AJ; and
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No fees are believed to be necessary. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to Deposit Account No. 09-0447.

Respectfully submitted,



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Levine et al.

Serial No: **10/675,872**

Filed: **September 30, 2003**

Title: **Method and Apparatus for Counting
Instruction and Memory Location Ranges**

Group Art Unit: **2192**

Intellectual Property
Law Department
International Business
Machines Corporation
11400 Burnet Road
Austin, Texas 78758

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. 1.56.

While this Supplemental Information Disclosure Statement may be "material" pursuant to 37 C.F.R. 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 C.F.R. 1.97(g) the filing of this Supplemental Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56 (b) exists.

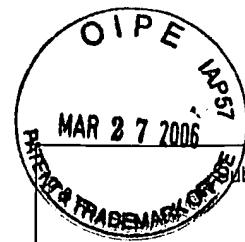
No item of information cited in this Supplemental Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in this Supplemental Information Disclosure Statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of this Supplemental Information Disclosure Statement.

In the event a fee is required in connection with the enclosed Supplemental Information Disclosure Statement, the Commissioner of Patents and Trademarks is authorized to charge Deposit Account No. 09-0447 for the necessary amount.

Respectfully submitted,



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known	
Application Number	10/675,872
Filing Date	09/30/2003
First Named Inventor	Levine et al.
Examiner Name	Vo, Ted T.
Art Unit	2192
Attorney Docket No.	AUS920030487US1

FOREIGN PATENT DOCUMENTS

Examiner Initial	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE

Examiner Initial	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
AH	TANENBAUM, "Structured Computer Organization", 1984, Prentice-Hall, Inc., 2 nd Edition, pp. 10-12.	
AI	TORRELLAS et al., "False Sharing and Spatial Locality in Multiprocessor Caches", June 1994, IEEE Transactions on Computers, Vol. 43, No. 6, pp. 651-663.	
AJ	ROTHMAN et al., "Analysis of Shared Memory Misses and Reference Patterns", 2000, IEEE, pp. 187-198.	

Examiner:

Date Considered:

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